Description

Method for the production of a memory cell, memory cell
and memory cell arrangement

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The invention relates to a method for producing a
memory cell, to a memory cell and to a memory cell
arrangement.

10   In view of the rapid development in computer
technology, there is a continued demand for
increasingly denser and inexpensive storage media.

From the prior art, a DRAM ("Dynamic Random Access
15   Memory") memory cell is known in which information is
coded in the state of charge of a capacitor. A DRAM has
the drawback of poor scalability. In addition, a DRAM
memory needs to be repeatedly refreshed, which is a
drawback in terms of the power balance. Furthermore,
20   stored information is lost from a DRAM when the power
supply is disconnected.

In the case of the SRAM ("Static Random Access Memory")
memory cell, a multiplicity of transistors are
25   connected together to store information. An SRAM has
poor scalability, and stored information is lost when
the power supply is disconnected.

An MRAM ("Magnetic Random Access Memory") memory cell
30   is also known from the prior art. In the case of this
memory cell, information which is to be stored is
clearly stored in the state of magnetization of a
magnetizable region, with the electrical conductivity
of an MRAM memory being dependent on the state of
35   magnetization of the magnetizable region. However, with
continued scaling of an MRAM, problems arise with the
phenomenon of superparamagnetism. The superparamagnetic
limit means that MRAM memories have only poor

scalability. In addition, only a small signal can be measured between the two memory states. Furthermore, difficulties arise when reading an MRAM memory cell arrangement, and reading normally requires the
5   provision of complex diodes.

An FeRAM memory cell is a modification of a DRAM memory cell in which the capacitor dielectric used is a ferroelectric layer. An FeRAM also has poor scalability
10 and can be produced only with a high level of complexity.

Other memory cells known from the prior art are an EEPROM ("Electrically Erasable and Programmable Read
15 Only Memory") and an NROM ("Nitrided Read Only Memory"). The two memory cells have only poor scalability, and high reading and programming voltages are required.

20 Most of the known memory cells are based on the introduction of electrons into a memory area. However, electrons tend to equalize the charge and therefore to flow out of the memory area, which means that memory information may be lost. Hence, sufficiently long
25 retention times can be achieved only with difficulty with such memory cells.

[1] describes an experiment in which a tunnel microscope ("Scanning Tunneling Microscope", STN) is
30 used to bring a silver sulfide tip within a few nanometers of a platinum substrate, and a suitable voltage is applied between the silver sulfide tip and the platinum substrate in order to form a quantum point contact between the silver sulfide tip and the platinum
35 substrate.

This experiment is described below with reference to figure 1A and figure 1B.

The first experimentation arrangement 100 shown in figure 1A contains a platinum substrate 101 which is arranged at a distance of a few nanometers from a
5   silver sulfide tip 102 using a tunnel microscope. As shown in the first experimentation arrangement 100, applying a first voltage 103 between the platinum substrate 101 and the silver sulfide tip 102 with an arithmetic sign which is such that the substrate 101 is
10   negatively charged with respect to the silver sulfide tip 102 results in silver atoms leaving the silver sulfide tip, which forms a quantum point contact 104 made of silver material. The electrochemical reactions taking place in this process are likewise shown in
15   figure 1A. Atomic silver material from the silver sulfide tip 102 is ionized to form positively charged silver ions on account of the arithmetic sign of the first voltage 103, whereas positively charged silver ions on the quantum tunnel contact between the platinum
20   substrate 101 and the silver sulfide tip 102 are reduced to form elemental silver. This results in the tunnel barrier between the platinum substrate 101 and the silver sulfide tip 102 being bridged.

25   The text below refers to the second experimentation arrangement 110 from figure 1B to explain what happens when a second voltage 111 is applied between components 101, 102, with the second voltage 111 having the opposite polarity from the first voltage 103. In this
30   operating state, the atomic silver of the quantum point contact 104 is ionized to form positively charged silver, which means that the quantum point contact 104 is taken back and there is no longer any electrical contact between the platinum substrate 101 and the
35   silver sulfide tip 102. Ionized silver from the silver sulfide tip 102 on the negative pole of the voltage source for producing the second voltage 111 is reduced to form atomic silver.

The formation of the quantum point contact 104 to bridge the components 101, 102 alters the electrical resistance of the arrangement comprising components
5   101, 102, as figure 2 shows.

Figure 2 shows a graph 200 along whose abscissa 201 an electrical voltage applied between the platinum substrate 101 and the silver sulfide tip 102 is
10   plotted. Along the ordinate 202, the value of the measured nonreactive resistance is plotted logarithmically. In a scenario which corresponds to the first experimentation arrangement 100, electrically conductive contact exists between the platinum
15   substrate 101 and the silver sulfide tip 102, which means that the arrangement comprising components 101, 102 has a low value for the nonreactive resistance. In a scenario which corresponds to the second experimentation arrangement 110, the quantum point
20   contact 104 has been taken back, which means that the platinum substrate 101 is electrically decoupled from the silver sulfide tip 102, and the arrangement comprising components 101, 102 has a low value for the nonreactive resistance. In the latter state, only a
25   small tunnel current can flow between components 102 and 102.

[2] discloses that aliphatic and aromatic self-assembled monolayers can be used as organic dielectrics
30   between two components which are intended to be arranged at a distance of a few nanometers from one another.

[3] discloses a vertical transistor for a DRAM memory
35   cell.

[4] to [10] disclose memories in which a chalcogenide is arranged between a first electrode and a second

electrode. The application of an electrical voltage
between the two electrodes allows a dendrite to grow or
regress through the chalcogenide.

5   However, a drawback of the memory cells known from [4]
to [10] is that a sufficiently high on/off ratio for
the memory cells can be achieved only using a large
volume of material. In addition, the growth of the
dendrite through the chalcogenide material means that
10   it is not possible to achieve a sufficiently fast
reading time and writing time for the memory cells.

[11] discloses a microelectronic programmable apparatus
and a method for forming and programming said
15   apparatus.

[12] discloses electrochemically current sources,
particularly lead storage batteries.

20   The invention is based on the problem of specifying a
method for producing a memory cell, a memory cell and a
memory cell arrangement which have improved properties
over the memory cells which are known from the prior
art.
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The problem is solved by a method for producing a
memory cell, by a memory cell and by a memory cell
arrangement having the features claimed in the
independent patent claims.

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The method for producing a memory cell involves a first
electrically conductive region being produced in or on
a substrate. In addition, a second electrically
conductive region is produced at a prescribed distance
35   from the first electrically conductive region such that
a cavity is formed between the first and second
electrically conductive regions. The first and second
electrically conductive regions are set up such that

upon application of a first voltage to the electrically
conductive regions a structure which at least partially
bridges the distance between the electrically
conductive regions is formed from material from at
5   least one of the electrically conductive regions. In
addition, the first and second electrically conductive
regions are set up such that upon application of a
second voltage to the electrically conductive regions
material from a structure which at least partially
10 bridges the distance between the electrically
conductive regions is taken back.

The inventive memory cell has a substrate and a first
electrically conductive region produced in or on the
15 substrate. In addition, the memory cell contains a
second electrically conductive region which is arranged
at a prescribable distance from the first electrically
conductive region such that a cavity is formed between
the first and second electrically conductive regions.
20 The first and the second electrically conductive region
are set up such that upon application of a first
voltage to the electrically conductive regions a
structure which at least partially bridges the distance
between the electrically conductive regions is formed
25 from material from at least one of the electrically
conductive regions. The first and the second
electrically conductive region are also set up such
that upon application of a second voltage to the
electrically conductive regions material from a
30 structure which at least partially bridges the distance
between the electrically conductive regions is taken
back.

In addition, the invention provides a memory cell
35 arrangement having a plurality of memory cells with the
features described above.

A basic idea of the invention can be seen in that a

memory cell is provided which can store information by
virtue of a first and a second electrically conductive
region jointly having either a high-resistance
structure (for example information with the logic value
5   "1") or a low-resistance structure (for example
information with a logic value "0"), the memory cell
being able to be switched reversibly between the two
states. If the two electrically conductive regions are
arranged at the prescribed tunnel spacing from one
10   another, which is formed by means of the defined
cavity, only a small tunnel current can flow between
the two electrically conductive regions, and the memory
cell assumes a high value for the nonreactive
resistance. If a structure which bridges the
15   electrically conductive regions is formed between the
two electrically conductive regions, however, the
arrangement has a significantly lower resistance.

In line with the invention, the bridging structure
20   between the electrically conductive regions is formed
or taken back over the cavity which is produced. The
growth or regression of the bridging structure can thus
be achieved at a much higher rate or at lower
electrical reading/writing voltages than in the case of
25   the memory cells described in [4] to [10], in which a
dendrite needs to grow through a solid-state layer. The
invention thus allows a much shorter reading and
writing time.

30   Unlike many memory cells known from the prior art (e.g.
DRAMs, SRAMs, FeRAMs, EEPROMs, NROMs etc.), the
inventive memory cell is not based on the storage of
slightly volatile electrical charge carriers, but
rather on forming or taking back a solid-state
35   structure to bridge the cavity between the electrically
conductive regions, which clearly corresponds more to a
mechanical relay on the nanometer scale. The memory
information is thus stored much more securely in the

inventive memory cell, which results in a high
retention time.

In addition, with a continued increase in the scale of
integration for memory cells, a memory cell in which
the memory information is stored in the form of
electrically charge carriers is subject to fundamental
physical problems. The long range of the Coulomb
interactions means that charge carriers in adjacent
memory cells, for example, can interact in unwanted
fashion, which means that the memory information may be
lost or manipulated in unwanted fashion. By contrast,
the inventive memory cell is a scalable memory cell
whose principle is not based on storing charge
carriers, which avoids the unwanted interaction effects
discussed above.

Since the cavity between the two electrically
conductive regions can be reduced into the angstrom
range and below (can clearly be produced as a quantum
point contact), the inventive memory cell arrangement
can be realized with a storage density of 60 terabits
per square inch and more in the case of a simple planar
arrangement. If the inventive memory cells are stacked
in three dimensions above one another, which is
possible on account of the layer architecture chosen,
then the storage density can be increased into the
pentabit range and above.

The inventive memory cell also has the advantages that
it is possible to write to it and read from it with
short times and small voltages, can be written to a
plurality of times, is nonvolatile and can be operated
under low power and low voltage demands. Thus, a supply
voltage of approximately 100 mV may be sufficient for
the inventive memory cell.

The use of a vacuum cavity (or a cavity filled merely

with gas) achieves a particularly high on/off ratio for
the nonreactive resistance values in the two operating
states of the memory cell (bridging structure
grown/bridging structure regressed). The use of a
5   tunnel contact allows an exponential characteristic and
thus a high level of reliability for the stored
information.

A core aspect of the invention may thus be seen in the
10 provision of a cavity produced between two electrode
regions without solid or liquid filling material (apart
from possible residual gas in the cavity), whose tunnel
spacing, preferably in the range of one nanometer, can
be changed up to a quantum point contact i.e. full
15 bridging of the cavity (for example using moving ions
in a solid-state electrolyte).

A multiplicity of such tunnel contacts, which each form
a memory cell, may be used to construct a memory cell
20 arrangement (in similar fashion to an MRAM). To read
stored information, it is possible to resort to the
reading principles of an MRAM, for example. Below each
memory cell in a memory cell arrangement, there may
also be a selection transistor or another selection
25 element which can be actuated by means of word lines
and bit lines and thus permits targeted reading of a
particular memory cell. In a crossover region between
two interconnects which are arranged at right angles to
one another, for example, it is possible to induce a
30 solid-state reaction, as described above with reference
to figure 1A and figure 1B.

It is thus possible for two electrodes, for example one
made of silver sulfide (Ag_2S) and the other made of
35 platinum or gold, to be arranged at a distance of
typically between 0.5 nm and 5 nm from one another, as
a result of which the two electrodes can interact with
one another through a material-free (vacuum) tunnel

barrier. If an electrical potential which is negative
with respect to the silver sulfide electrode is applied
to the platinum electrode, then electrodes can tunnel
through the tunnel spacing and can neutralize silver
5   ions in the Ag_2S electrode to form elemental silver,
which silver is then deposited on the surface of the
silver sulfide electrode and forms one or more quantum
point contacts. If the voltage has the opposite
polarity, the silver ions are ionized and migrate back
10   into the Ag_2S electrode, which means that an operating
state with a high nonreactive resistance is again
obtained.

An important aspect of the invention can therefore be
15   seen in the reproducible production of an adjustable
tunnel spacing between two electrically conductive
regions (for example two electrodes).

Preferred developments of the invention can be found in
20   the dependent claims.

In the method for producing a memory cell, the
prescribed distance between the first and second
electrically conductive regions can be formed by
25   producing an auxiliary structure of prescribed
thickness on the first electrically conductive region
and removing the auxiliary structure after the second
electrically conductive region is formed. An auxiliary
or sacrificial structure of a prescribable thickness
30   can thus be used to stipulate and set the geometry of
the subsequently produced cavity accurately. Expressed
another way, the auxiliary structure serves as a spacer
between the electrically conductive regions.

35   Preferably, the auxiliary structure used is a self-
assembled monolayer, as described in [2], for example.
A self-assembled monolayer may be, by way of example,
an organic molecule comprising a carbon chain of

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adjustable length and a sulfur ion linked thereto. If the gold/sulfur coupling, which is particularly beneficial in terms of the coupling chemistry, for example, is used then the self-assembled monolayer's

5   sulfur ion can be coupled to one of the electrically conductive regions, which means that the two electrically conductive regions can be arranged from one another at a distance in the nanometer range. Since, in particular, the length of the carbon chain

10 can be adjusted more or less arbitrarily, it is possible to define the distance between the two electrically conductive regions using self-assembled monolayers as far as an accuracy in the angstrom range and below. After the second electrically conductive

15 region has been produced on the self-assembled monolayer, the self-assembled monolayer can be removed using a selective etching method, which produces the cavity. The use of self-assembled monolayers (SAMs), which can also be called self-organizing monolayers,

20 allows a defined distance between the two electrically conductive regions to be prescribed to an accuracy of 100 pm and below, with a high level of reproducibility.

As an alternative to using a self-assembled monolayer,

25 the auxiliary or sacrificial structure can be produced using an atomic layer deposition method (ALD method). This method allows the defined deposition of a layer with a thickness which can be adjusted down to the accuracy of an atomic layer, i.e. down to an accuracy

30 of a few angstroms.

Alternatively, the auxiliary structure may be produced using a molecular beam epitaxy method (MBE method).

35 The prescribed distance between the two electrically conductive regions is preferably between approximately 0.5 nm and approximately 5 nm, and with further preference between approximately 0.6 nm and

approximately 2 nm. Such distances allow a bridging
structure to form or regress sufficiently quickly,
which means that fast programming and erasure times are
achieved.

The inventive method allows the first electrically
conductive region to be produced as a first
interconnect, and the second electrically conductive
region to be produced as a second interconnect, which
interconnects can be produced so as to run at right
angles to one another. Clearly, the crossover region
for a first and a second interconnect, isolated by the
tunnel contact, forms a memory cell based on the
invention.

The text below describes the inventive memory cell in
more detail. Refinements of the method for producing a
memory cell also apply to the memory cell, and vice
versa.

In the case of the inventive memory cell, the substrate
may be a semiconductor substrate, preferably a silicon
substrate such as a silicon wafer or a silicon chip.

The first or the second electrically conductive region
(particularly that electrically conductive region from
which a bridging structure can grow to the other
electrically conductive region) can comprise a solid-
state electrolyte, a glass comprising metal ions, a
semiconductor comprising metal ions or a chalcogenide.
A chalcogenide can be understood to be a material which
comprises an element from the sixth main group in the
periodic table of the elements, particularly sulfur,
selenium and/or tellurium. Preferably, the first or the
second electrically conductive region comprises a
chalcogenide material and a metal material. The
chalcogenide material can be selected from the group
comprising arsenic, germanium, selenium, tellurium,

bismuth, nickel, sulfur, polonium and zinc. The metal
material can be selected from the first or second main
group in the periodic table of the elements, with
silver, copper or zinc being preferred.

By way of example, the first or the second electrically
conductive region may comprise silver sulfide, or
alternatively arsenic sulfide, germanium sulfide or
germanium selenide.

The first or the second electrically conductive region
(particularly that electrically conductive region to
which a bridging structure can grow from the other
electrically conductive region) may comprise metallic
material, such as silver, gold, aluminum and/or
platinum.

Of particular advantage is a material combination in
which one of the electrically conductive regions is
produced from gold material, silver material or copper
material, and the auxiliary structure used is a self-
assembled monolayer with a sulfur end group. In this
case, it is possible to use the beneficial gold/sulfur
coupling chemistry, which also acts with the materials
silver and copper in similar fashion.

The text below gives a more detailed description of the
inventive memory cell arrangement containing inventive
memory cells. Refinements of the memory cell also apply
to the memory cell arrangement comprising memory cells.

The memory cells may be arranged essentially in matrix
form. By way of example, first interconnects can be
produced as first electrically conductive regions in a
first direction and second interconnects can be
produced as second electrical conductive regions in a
second direction. Each crossover region between one of
the first interconnects and one of the second

interconnects may then contain a memory cell based on the invention if the first or second interconnects are arranged from one another at a distance which corresponds to a tunnel spacing.

For at least some of the memory cells in the memory cell arrangement, selection elements for selecting a memory cell may be produced in and/or on the substrate. The selection elements are preferably field effect transistors, and with further preference vertical field effect transistors. The selection elements may be used as switching elements, which means that it is possible to detect the flow of current through a memory cell selected by applying an electrical voltage to the gate region of a field effect transistor and therefore to read the information content stored therein.

Exemplary embodiments of the invention are shown in the figures and are explained in more detail below.

In the figures:

Figures 1A and 1B show experimentation arrangements based on the prior art,

Figure 2   shows a graph showing a voltage/resistance characteristic for the experimentation arrangements shown in figure 1,

Figures 3A to 3D show layer sequences at different times during a method for producing a memory cell in line with a preferred exemplary embodiment of a invention,

Figure 4   shows a memory cell arrangement in line with a preferred exemplary embodiment of the invention,

Figure 5   shows a memory cell in line with a preferred
          exemplary embodiment of the invention, and

Figure 6   shows a memory cell in line with another
          preferred   exemplary   embodiment   of   the
          invention.

Components which are the same or similar in different
figures have been provided with the same reference
numerals.

The illustrations in the figures are schematic and not
to scale.

The text below refers to figure 3A to figure 3D to
describe a method for producing a memory cell in line
with the preferred exemplary embodiment of the
invention.

To obtain the layer sequence 300 shown in figure 3A, a
silicon oxide layer 302 (which is approximately 100 nm
thick in this exemplary embodiment) is deposited onto a
silicon substrate 301 in which evaluation or switching
electronics (for example amplifiers, selection
transistors etc.) may already have been produced
beforehand. A photoresist layer 303 is deposited onto
the silicon oxide layer 302. Using a lithography method
and a dry-etching method, a trench 305 is made in the
silicon oxide layer 302 or in the photoresist layer
303. After the etching, the material of the photoresist
layer 303 is not incinerated, but rather is subjected
to a wet-etching step using buffered hydrofluoric acid
(HF), such that slight underetching of the photoresist
303 is obtained. Next, a directional vapor deposition
or sputtering method is used to deposit a titanium
layer which is approximately 10 nm thick in the trench
305 (not shown in the figure). Gold material 304 is
then deposited up to a prescribed thickness, which is

chosen such that the trench 305 made in the silicon oxide layer 302 is just filled. This also deposits gold material 304 onto the surface of the photoresist 303.

5   To obtain the layer sequence 310 shown in figure 3B, a liftoff method is used to remove material of the photoresist 303 and of the share of the gold material 304 which is produced thereon, so that a gold electrode 311 remains in the trench 305. The layer sequence

10   obtained in this manner is subjected to treatment in H_2 or O_2 plasma. Next, an SAM layer (self-assembled monolayer) 312 of a prescribed thickness (i.e. molecular length) is put onto the gold electrode 311. The SAM layer 312 comprises molecules which have a

15   carbon chain whose one end portion holds a group containing sulfur. This sulfur group can dock on the gold material of the gold electrode 311 in defined fashion, so that the SAM layer 312 is produced in the manner shown in figure 3B with good physical location.

20   By selecting the length of the molecules in the SAM layer 312, it is possible to set the thickness of the subsequently produced tunnel cavity exactly. When the SAM layer 312 has been deposited, the resultant layer sequence is covered with a germanium sulfide layer

25   which is approximately 10 nm thick, and is then sputtered with a silver layer which is approximately 1 nm to 5 nm thick. The resultant layer sequence is subjected to UV radiation, which drives silver ions into the germanium sulfide layer. The resultant layer

30   sequence can be sputtered again with gold, silver or platinum in order to increase the electrical conductivity or the mechanical robustness of the top layer. Optionally, an additional silver sulfide layer which is approximately 10 nm thick can be vapor

35   deposited and possibly reinforced. This results in the chalcogenide electrode 313 produced on the SAM layer 312.

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The text below describes how the layer sequence 320 shown in figure 3C is obtained. It should first be noted that the views in figure 3A, figure 3B, figure 3D are cross-sectional views which are different than the
5   cross-sectional view in figure 3C. Figure 3C shows a development of the layer sequence 310 which is shown in figure 3B, taken along a sectional line I-I' which is shown in figure 3B.

10   To obtain the layer sequence 320 shown in figure 3C, the chalcogenide electrode 313 is patterned to form an interconnect. This is done using a further resist mask (not shown in the figure) and subsequent dry etching. This exposes the SAM layer 312. The SAM layer 312 is
15   then removed using a solvent and a temperature increase with possibly subsequent hydrogen plasma treatment, which forms the material-free tunnel contact or cavity 321.

20   The layer sequence 320 is a memory cell in line with a preferred exemplary embodiment of the invention.

     Figure 3D shows the memory cell from figure 3C in a view which corresponds to that shown in figure 3A and
25   figure 3B.

     It should be noted that the memory cell shown in figure 3C and figure 3D can be covered with silicon oxide produced using a plasma method. The arrangement
30   obtained can be planarized, e.g. using a CMP ("Chemical Mechanical Polishing") method. A further layer of memory cells can then be produced on the memory cell or memory cell arrangement which has been made. This allows large scale 3D integration.

35
     The text below refers to figure 3D to explain the functionality of the memory cell stored there.

A description will first be given of how information can be programmed into the memory cell. If a positive electrical potential is applied to the chalcogenide electrode 313 and a negative electrical potential is

5   applied to the gold electrode 311 then a silver bridging structure grows from the chalcogenide electrode 313 and bridges the cavity 321 (which is a few nanometers thick) between the gold electrode 311 and the chalcogenide electrode 313. If the value of the

10 electrical current is now measured for a reading voltage between the electrodes 311, 313, it will be high on account of the low-resistance configuration caused by bridging the cavity 321 with the bridging structure. If the polarity of the previously applied

15 voltage between the electrodes 311, 313 is reversed, so that the positive potential is applied to the gold electrode 311, then the dendrite or the bridging structure regresses, so that the cavity 321 forms a tunnel spacing between electrodes 311, 313. The flow of

20 current when the reading voltage is applied is now smaller than in the case in which a bridging structure is formed.

The operating states "high nonreactive resistance" or

25 "low nonreactive resistance" can be identified by the logic values "1" and "0" (or vice versa), for example. The memory information is thus clearly coded in the respective value of a memory cell's nonreactive resistance.

30

The text below refers to figure 4 to describe a memory cell arrangement 400 in line with a preferred exemplary embodiment of the invention.

35 The memory cell arrangement 400 is formed from a multiplicity of gold bit lines 401 running in a first direction and from a multiplicity of chalcogenide word lines 402 (comprising silver sulfide) running

essentially at right angles thereto. Each crossover
region between a gold bit line 401 and a chalcogenide
word line 402 contains a cavity (not shown in figure 4)
which forms a memory cell of the invention together
5   with adjoining regions of the associated gold bit line
401 and of the associated chalcogenide word line 402.
The cavities in the crossover regions between gold bit
lines 401 and chalcogenide word lines 402 are in turn
formed by removing a previously applied SAM (self-
10   assembled monolayer) layer.

The text below refers to figure 5 to describe a memory
cell 500 in line with a preferred exemplary embodiment
of the invention.

15

The memory cell shown in figure 5 has a first electrode
501 and a second electrode 502, between which
electrodes 501, 502 a cavity 503 is formed. The first
and second electrodes 501, 502 are set up such that
20   upon application of a first voltage between the
electrodes 501, 502 a structure which bridges the
cavity 503 is formed from material from one of the
electrodes 501, 502. In addition, the two electrodes
501, 502 are set up such that upon application of a
25   second voltage, whose polarity is opposite to that of
the first voltage, between the electrodes 501, 502
material from a structure which bridges the cavity 503
between the electrodes 501, 502 is taken back, which
electrically decouples the electrodes 501, 502 from one
30   another over the cavity.

In other words, for a fixed voltage between the
electrodes 501, 502, the value of the electrical
current is dependent on whether or not the cavity 503
35   is bridged by a bridging structure. Components 501 to
503 thus form the core region of the memory cell 500,
with a multiplicity of memory cells 500 being able to
be arranged in a memory cell arrangement in a similar

manner to the one shown in figure 4, for example. In this case, it is necessary to be able to write the memory information to a particular memory cell, or to read it therefrom, in defined fashion. This is done using a vertical field effect transistor in the exemplary embodiment shown in figure 5. To be precise, figure 5 shows two vertical field effect transistors, one of which is associated with the components 501 to 503. The other field effect transistor, which is of similar design to the field effect transistor associated with the components 501 to 503, can be used to couple to another memory cell.

The second electrode 502 is coupled to a first source/drain region 504 in the vertical field effect transistor. Arranged between the first source/drain region 504 and a second source/drain region 505 is a channel region (not shown in figure 5) of the vertical field effect transistor. The channel region is surrounded by a surrounded gate 506, with the surrounded gate 506 being decoupled from the channel region by means of a gate-insulating region (not shown).

The text below explains the functionality of the memory cell 500. If the cavity 503 between the electrodes 501, 503 is bridged in a first operating state, the arrangement of components 501 to 503 has a low value for the nonreactive resistance. The application of a voltage to the surrounded gate region 506 makes the channel region conductive on account of the field effect, and a flow of electric current between the source/drain regions 504, 505 is possible. When a fixed voltage is applied between the first electrode 501 and the second source/drain region 505, the value of the electrical current which flows is a measure of whether or not the cavity 503 is bridged by a bridging structure. The value of the electrical current is thus

higher in the scenario described than in a complementary scenario in which the cavity 503 is free of any bridging structure. In other words, by applying an electrical potential to the surrounded gate region
5   506 and a potential between the first electrode 501 and the second source/drain region 505 it is possible to read the memory cell.

By applying a sufficiently high electrical voltage of
10 prescribable polarity between the first electrode 501 and the second gate region 505, a bridging structure can be grown or taken back in the cavity 503.

It should be noted that the inventive memory cell is
15 not limited to two electrodes.

Figure 6 shows a memory cell 600 in line with another exemplary embodiment of the invention, in which a first chalcogenide electrode 601 and a second chalcogenide
20 electrode 602 are provided. In addition, a silver electrode 603 is arranged at a prescribed distance "d" from the chalcogenide electrodes 601, 602. By applying a suitable voltage between at least one of the chalcogenide electrodes 601, 602 and the silver
25 electrodes 603, it is possible to grow a bridging structure 604 jointly starting from the chalcogenide electrodes 601, 602, in order to produce coupling to the silver electrode 603.

30 Accordingly, arbitrarily more complicated arrangements of electrodes are possible, because it is possible to produce reversible coupling selectively, for example just between electrodes 601 and electrodes 603 or just between electrodes 602 and 603. This means that
35 couplings can be formed and removed again in circuits reversibly at microelectronic level.

It should also be noted that the inventive memory cell

may also be used as a logic element, with logic being
able to be written to an appropriate logic element
reversibly.